

Industry Forum Program—Jan 3-5, 2005

January 3rd, 2005

Session 1E (11:00 AM - 1:00 PM)		
Venue: Crystal East		
	Title	Speaker
11:15	Introduction to Industry Forum	S S S P Rao, IIT Mumbai
11:25	Cadence University Program 2005-What's new and exciting!	Zahida Vaseem
11:45	Intel Advance Switching Based on PCI Express	Sam Sanyal
12:05	Mentor Graphics Achieving Very High Test Quality in the Nanometer Era	Nilanjan Mukherjee
12:25	TI SoC Design Challenges - TI perspective	Mahesh Mehendale
12:45	Agere Realizing Personal Broadband through Unbreakable Access and Differentiated Traffic Management	Deepak Kataria / Nagi Naganathan
13:15 Lunch		

Session 2E (2:30 PM - 4:30 PM)		
Venue: Mandarin		
14:30	nSys nSys on Accelerating Designs	Jitendra Puri
14:50	Synopsys Corporate Overview of Synopsys	Shruti Vij
15:10	Logicvision Methods to Accelerate Yield Learning	Ashish Gupta
15:30	Natsem National Semiconductor Corporate and IPDC	Ashok Kumar
15:50	Sequence Next generation EDA tools to enable power-aware nanometer SOCs	Piyush Sancheti
16:00	CG-Corel GDS -Based Parasitic Extraction a necessity for Advanced Process Technology	Adhir Upadhyay
	CG-Corel How to Utilize distributed processing power to get significant performance improvement for DRC and LVS	Adhir Upadhyay
16:30 Afternoon Tea		

January 4th, 2005

Session 3E (11:00 AM - 1:00 PM)

Venue: Incognito

	Title	Speaker
11:00 Centilium	Passive Optical Networks	M N Kumar
11:20 CoWare	Embedded Software development in the Platform Context	Sanjay Chakravarty
11:40 Interra	Accelerate Product Deployment Using ASIC/SoC, Memory Design and Verification Services	Saikat Bandyopadhyay
12:00 Tensilica	Configurable Processors for SoCs	Ashish Dixit
12:20 Transwitch	Transwitch presentation	Prosit Mukherjee
12:40 Softjin	Ensuring Improved QoR through Optimal Design Flow	Niket Vakharia
12:50 Alumnus	Surviving Odds---All Odds	Arindam Mukherjee
13:00 Lunch		

Session 4E (2:15 PM - 4:15 PM)

Venue: Incognito

14:15 Alliance Semiconductors	Alliance addresses portable market with its state of the art mixed signal products	Jayanta Lahiri
14:35 Trident Techlabs	Silvaco Productline	Manav Tyagi
14:55 Mechatronics	PCB Design Issues When Designing With Multimillion Gate FPGA	Rakesh Mehta
15:15 Open-Silicon	Open Model : Enabling Innovation in ASICs	Satya Gupta
15:35 Infineon	Markets, Products & Technology: Do They Fit Together?	Vijay Mehra
16:05 Infineon	Modeling of ASIP and Customization of the Tools	Srinivas B P
16:15 Afternoon Tea		

January 5th, 2005

Session 5E (11:00 AM - 1:00 PM)

Title

Speaker

Venue: Incognito

11:00	Magma-DA	Magma- Meeting your Nanometer design goals	Ricky Bedi
11:20	Virage Logic	Virage Logic - Accelerating Silicon Success	Yervant Zorian
11:40	eInfochips Ltd	VeriSuite - eInfochips Verification Package	Rohit Dubey
12:00	Xilinx-CMC	Work Environment at Xilinx-CMC India Development Center "WE@XIDC"	S.S.S.P.Rao
12:30	National Instruments	Virtual Instrumentation in VLSI & Semiconductors	Sanchit Bhatia
12:40	Govt. of India	Design and Development of Digital Hearing Aid	R. Ravindra Kumar

13:00 Lunch

Session 6E (4:15 PM - 6:15 PM)

Venue: Crystal Central

16:15	IIT, Kharagpur	Advanced VLSI Design Laboratory	Pallab Dasgupta
16:35	Atrenta	Atrenta - Company Update	Puranjan Mukhopadhyay
16:55	Zenasis	Breaking the ASIC Speed Barrier	Rob Roy
17:15	Panel Discussion: Indian Industry- Academia Interaction	How do we go from Standoff to Stable Marriage?	