

## REGISTRATION FORM FOR DELEGATES FROM INDIA

Name: Mr./Ms./Dr./Prof. \_\_\_\_\_

Company/Affiliation: \_\_\_\_\_

Address: \_\_\_\_\_

City: \_\_\_\_\_ Postal Code: \_\_\_\_\_

Phone: \_\_\_\_\_ Mobile : \_\_\_\_\_ Fax: \_\_\_\_\_ Email: \_\_\_\_\_

**Note:** All advance registration must be received by November 30, 2004 to avail of discounted registration fees.

**Membership details** (tick [] as appropriate)

Member: VSI [] IEEE [] ACM []

Membership No: \_\_\_\_\_

### A. Registration Fees (Please TICK [] the amount applicable)

Registration Fees		Members: Amount (INR)		Non-Members: Amount (INR)	
Conference (Jan. 3-5)		Up to Nov 30	From Dec 1	Up to Nov 30	From Dec 1
		5500 [ <input type="checkbox"/> ]	6500 [ <input type="checkbox"/> ]	7000 [ <input type="checkbox"/> ]	8000 [ <input type="checkbox"/> ]
Tutorials (Jan. 6 - 7)	1 day	2000 [ <input type="checkbox"/> ]	2500 [ <input type="checkbox"/> ]	2500 [ <input type="checkbox"/> ]	3000 [ <input type="checkbox"/> ]
	2 days	3500 [ <input type="checkbox"/> ]	4500 [ <input type="checkbox"/> ]	4500 [ <input type="checkbox"/> ]	5500 [ <input type="checkbox"/> ]
<b>Total</b>					

The conference fee includes the registration kit, CD-ROM containing proceedings of this conference and **archives of past years**, lunch, coffee service, high-tea and banquet dinner.

### Tutorial Program

(Please enter your order of preference [1<sup>st</sup>, 2<sup>nd</sup>, 3<sup>rd</sup>] next to the tutorial codes for each day)

Jan 6, 2005 (T1, T2, T3, T4 run in parallel)		Jan 7, 2005 (T5, T6, T7, T8 run in parallel)	
<b>T1</b> [ <input type="checkbox"/> ]	Power-Aware reliable microprocessor design	<b>T5</b> [ <input type="checkbox"/> ]	Test Methodologies in the Deep Sub-micron Era - Analog and RF
<b>T2</b> [ <input type="checkbox"/> ]	High-Speed Interconnect Technology: On-Chip and Off-Chip	<b>T6</b> [ <input type="checkbox"/> ]	Recent Advances in Verification, Equivalence Checking & SAT-Solvers
<b>T3</b> [ <input type="checkbox"/> ]	Testing Nanometer Integrated Circuits: Myths, Reality and the Road Ahead	<b>T7</b> [ <input type="checkbox"/> ]	<b>A:</b> Compact MOSFET Models for Low Power CMOS Design <b>B:</b> Physics and Technology: Towards Low-Power DSM Design
<b>T4</b> [ <input type="checkbox"/> ]	SoC Design Methodology: A Practical Approach	<b>T8</b> [ <input type="checkbox"/> ]	Architectural, System Level and Protocol Level Techniques for Power Optimization for Networked Embedded Systems

The Tutorial fee includes tutorial material, lunch, and coffee service.

**B. Hardcopy of this year's proceedings (Please TICK []):** INR 4000/- []

**C. Accommodation charges (if applicable) :**  
(Please see Accommodation Guidelines on the next page)

Choice of Hotel : 1 <sup>st</sup> Choice : _____	Single Room [ <input type="checkbox"/> ] Double Room [ <input type="checkbox"/> ]
2 <sup>nd</sup> Choice : _____	Check in Date : _____
3 <sup>rd</sup> Choice : _____	Check out Date: _____
Amount of Advance: INR _____	No. of Nights : _____

**Total (A+B+C) = INR** \_\_\_\_\_

## Payment Modes

1. All payment by Participants from India may please be made in Indian Rupees. Remittance can be made by an account payee Demand Draft drawn in favour of "**VLSI TRUST 2005**" payable at HDFC Bank Ltd., Kolkata, India. In case companies are making group registration, the payment may be made by a single draft.

Demand Draft No \_\_\_\_\_ Dated: \_\_\_\_\_

Drawn on (Bank Name): \_\_\_\_\_

Amount Rs. \_\_\_\_\_

2. Your bank can also transfer the remittance to us by using the following SWIFT Code details of the conference Account.

Our Banker's details for remitting funds:

Bank Name	:	HDFC Bank Ltd.
A/c No. of HDFC Bank, Mumbai With Chase Manhattan	:	001-1-406717
Credit to VLSI TRUST 2005	:	2771000002747
CHIPS UID	:	5482390
SWIFT ID	:	CHASUS33

**Please forward a copy of the money transfer report to the Conference Secretariat**

## Accommodation Guidelines

- Please refer to the list of hotels on the Conference Website. These hotels have offered specially discounted rates for the Conference. This rate is valid only if the booking for the hotel and the advance payment for the period of your stay are received within 30-Nov-04.
- Please provide three choices for the hotel from the most preferred to least preferred. Best effort will be made to honor the choice as per the availability of rooms in your preferred hotel.
- The conference will transfer your advance amount to the hotel and issue a confirmation via e-mail. You will need to provide this confirmation at the time of check-in at the hotel. When you settle your final bill, the hotel will issue consolidated receipts.
- Cancellation should be intimated to the conference secretariat latest by 30-Nov-04 and will be governed by the respective hotel policy. Under most common terms of the hotels, cancellation after 30-Nov-04 will attract deduction of one day's tariff.
- Bank charges for refunding will be deducted from the refund amount.
- The normal hotel check-in and check-out time is 1200-hrs noon.

## All correspondence to be sent to:

Attrn: Mr Nand Gopal Chattopadhyay  
Conference Finance Chair  
**VLSI 2005 CONFERENCE SECRETARIAT**  
C/o. Interra Systems India (Pvt.) Ltd.  
2<sup>nd</sup> Floor, STP II Building, Salt Lake Electronics Complex  
Plot No. 53, Block DN, Sector V, Bidhannagar, Kolkata 700 091  
India.  
Phone: (91) (33) 2367 3600, Fax: (91) (33) 2367 3520

For registration related queries please write to: [vlsi05reg@vlsi-india.net](mailto:vlsi05reg@vlsi-india.net)  
For any other query please write to the organizers: [vlsi05org@vlsi-india.net](mailto:vlsi05org@vlsi-india.net)

Date: \_\_\_\_\_

Signature \_\_\_\_\_

Sponsored by:



VLSI Society of India (VSI)



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