

| <b>VLSI 2005: Program Matrix for Technical Sessions and Industry Forum</b> |                                       |                                 |   |   |                      |
|--|---------------------------------------|---------------------------------|---|---|----------------------|
|  | <b>CRYSTAL Combined</b>               | <b>Crystal East</b>             | <b>Hall Color Codes</b>                   | <b>Mandarin</b>                           | <b>Banquet Lawns</b> |
|  | <b>Crystal Central</b>                | <b>Crystal West</b>             |   | <b>Incognito</b>                          | <b>Break</b>         |
| <b>January 3, 2005</b>   |                                       |                                 |   |   |                      |
| <b>9:00</b>  | Inauguration of Conference            |                                 |   | Free                                      | Free                 |
| <b>9:30</b>  | Inaugural Keynote Address             |                                 |   | Free                                      | Free                 |
| <b>10:30</b>   | Inauguration of Technical Exhibition  |                                 |   | Free                                      | Free                 |
| <b>10:45</b>   | Morning Tea                           |                                 |   |   |                      |
| <b>11:15</b>   | 1A: Test I                            | 1B: Physical Design             | 1C: Embedded Systems                      | 1D: Low Power                             | 1E: Industry Forum   |
| <b>13:15</b>   | Lunch                                 |                                 |   |   |                      |
| <b>14:30</b>   | 2A: Formal Verification               | 2B: Nanotechnology and Biochips | 2C: Synthesis I                           | 2D: RF and Mixed Signal                   | 2E: Industry Forum   |
| <b>16:30</b>   | Afternoon Tea                         |                                 |   |   |                      |
| <b>17:00</b>   | Monday Afternoon Plenary Session      |                                 |   | Free                                      | Free                 |
| <b>18:30</b>   | Break                                 |                                 |   |   |                      |
| <b>19:00</b>   | Monday Banquet Speech                 |                                 |   | Free                                      | Free                 |
| <b>20:00</b>   | Dinner                                |                                 |   |   |                      |
| <b>January 4, 2005</b>   |                                       |                                 |   |   |                      |
| <b>8:30</b>  | Tuesday Morning Keynote Session       |                                 |   | Free                                      | Free                 |
| <b>10:30</b>   | Morning Tea                           |                                 |   |   |                      |
| <b>11:00</b>   | 3A: Signal Integrity and Crosstalk    | 3B: Process Variation           | 3C: Design Methodology                    | 3D: Placement and Routing                 | 3E: Industry Forum   |
| <b>13:00</b>   | Lunch                                 |                                 |   |   |                      |
| <b>14:15</b>   | 4A: Test II                           | 4B: Analog                      | 4C: Architecture                          | 4D: Power Estimation and Low Power Design | 4E: Industry Forum   |
| <b>16:15</b>   | Afternoon Tea                         |                                 |   |   |                      |
| <b>16:45</b>   | Panel Discussion                      |                                 |   | Free                                      | Free                 |
| <b>18:15</b>   | Break                                 |                                 |   |   |                      |
| <b>18:45</b>   | Conference Speeches & Awards          |                                 |   | Free                                      | Free                 |
| <b>19:30</b>   | Tuesday Banquet Speech                |                                 |   | Free                                      | Free                 |
| <b>20:30</b>   | Dinner                                |                                 |   |   |                      |
| <b>January 5, 2005</b>   |                                       |                                 |   |   |                      |
| <b>7:30</b>  | Breakfast                             |                                 |   |   |                      |
| <b>8:30</b>  | India Semiconductor Association Event |                                 |   | Free                                      | Free                 |
| <b>9:30</b>  | Wednesday Morning Keynote Session     |                                 |   | Free                                      | Free                 |
| <b>10:30</b>   | Morning Tea                           |                                 |   |   |                      |
| <b>11:00</b>   | 5A: Interconnect                      | 5B: Synthesis II                | 5C: Power-aware design and Thermal Issues | 5D: Technology                            | 5E: Industry Forum   |
| <b>13:00</b>   | Lunch                                 |                                 |   |   |                      |
| <b>14:15</b>   | Wednesday Afternoon Plenary Session   |                                 |   | Free                                      | Free                 |
| <b>15:45</b>   | Afternoon Tea                         |                                 |   |   |                      |
| <b>16:15</b>   | 6A: Test III                          | 6B: Algorithms and Applications | 6C: Posters                               | 6D: Posters and RSF                       | 6E: Industry Forum   |

## VLSI 2005: Program Matrix for Industry Forum

| VLSI 2005: Program Matrix for Industry Forum |   |           |                                      |           |  |
|--|---|-----------|--------------------------------------|-----------|--|
|  | CRYSTAL Combined                            |           | Hall Color Codes                     |           | Crystal Central                              |
|  | Mandarin                                    |           | Banquet Lawns                        |           | Crystal East                                 |
|  | Incognito                                   |           | Break                                |           | Crystal West                                 |
| Session                                      | January 3, 2005                             | Session   | January 4, 2005                      | Session   | January 5, 2005                              |
| <b>1E</b>                                    |   | <b>3E</b> |                                      | <b>5E</b> |  |
|  | <b>11:15</b> Introduction to Industry Forum |           | <b>11:00</b> Centilium               |           | <b>11:00</b> Magma-DA                        |
|  | <b>11:25</b> Cadence                        |           | <b>11:20</b> CoWare                  |           | <b>11:20</b> Virage Logic                    |
|  | <b>11:45</b> Intel                          |           | <b>11:40</b> Interra Systems         |           | <b>11:40</b> eInfochips                      |
|  | <b>12:05</b> Mentor Graphics                |           | <b>12:00</b> Tensilica               |           | <b>12:00</b> Xilinx-CMC                      |
|  | <b>12:25</b> Texas Instruments              |           | <b>12:20</b> TranSwitch              |           | <b>12:30</b> National Instruments            |
|  | <b>12:45</b> Agere Systems                  |           | <b>12:40</b> Softjin                 |           | <b>12:40</b> Govt. of India                  |
|  | <b>13:15</b> Lunch                          |           | <b>12:50</b> Alumnus Software        |           | <b>13:00</b> Lunch                           |
|  |   |           | <b>13:00</b> Lunch                   |           |  |
| <b>2E</b>                                    |   | <b>4E</b> |                                      | <b>6E</b> |  |
|  | <b>14:30</b> nSys                           |           | <b>14:15</b> Alliance Semiconductors |           | <b>16:15</b> Adv. VLSI Design Lab - IIT, KGP |
|  | <b>14:50</b> Synopsys                       |           | <b>14:35</b> Trident Techlabs        |           | <b>16:35</b> Atrenta                         |
|  | <b>15:10</b> LogicVision                    |           | <b>14:55</b> Mechatronics            |           | <b>16:55</b> Zenasis                         |
|  | <b>15:30</b> Natsem                         |           | <b>15:15</b> Open-Silicon            |           | <b>17:15</b> Panel: Industry/Academia        |
|  | <b>15:50</b> Sequence Design                |           | <b>15:35</b> Infineon                |           |  |
|  | <b>16:00</b> CG-CoreEI                      |           | <b>16:15</b> Afternoon Tea           |           |  |
|  | <b>16:30</b> Afternoon Tea                  |           |                                      |           |  |

## VLSI 2005: Program Matrix for Tutorials

| VLSI 2005: Program Matrix for Tutorials |  |   |  |   |
|---|--|---|--|---|
| <b>January 6, 2005</b>                  |  |   |  |   |
| <b>9:00</b>                             | T1: Power-Aware reliable microprocessor design                                 | T2: High-Speed Interconnect Technology: On-Chip and Off-Chip            | T3: Testing Nanometer Integrated Circuits: Myths, Reality and the Road Ahead | T4: SoC Design Methodology: A Practical Approach  |
| <b>10:30</b>                            | Morning Tea  |   |  |   |
| <b>11:00</b>                            | T1   | T2  | T3   | T4  |
| <b>12:30</b>                            | Lunch  |   |  |   |
| <b>13:30</b>                            | T1   | T2  | T3   | T4  |
| <b>15:00</b>                            | Afternoon Tea  |   |  |   |
| <b>15:30</b>                            | T1   | T2  | T3   | T4  |
| <b>January 7, 2005</b>                  |  |   |  |   |
| <b>9:00</b>                             | T5: Test Methodologies in the Deep Submicron Era - Analog, Mixed-Signal and RF | T6: Recent Advances in Verification, Equivalence Checking & SAT-Solvers | T7A: Compact MOSFET Models for Low Power Analog CMOS Design.                 | T8: Architectural, System Level and Protocol Level Techniques for Power Optimization for Networked Embedded Systems |
| <b>10:30</b>                            | Morning Tea  |   |  |   |
| <b>11:00</b>                            | T5   | T6  | T7A  | T8  |
| <b>12:30</b>                            | Lunch  |   |  |   |
| <b>13:30</b>                            | T5   | T6  | T7B: Physics and Technology: Towards Low-Power DSM Design                    | T8  |
| <b>15:00</b>                            | Afternoon Tea  |   |  |   |
| <b>15:30</b>                            | T5   | T6  | T7B  | T8  |