RESUME OF DEBASRI SAHA

Personal:

Name:	**DEBASRI SAHA**
Sex:	Female
Marital Status:	Single
Nationality:	Indian

Educational:

- Pursuing Ph.D. in Computer Science as a Research Fellow (Institute Scholar) in Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata.
- Completed M. Tech in Computer Science and Engg. from University of Calcutta in 2006 with 83.4% marks and university rank 1st.
- Completed B. Tech in Computer Science and Engg. from University of Calcutta in 2004 with 75.4% marks.
- Completed B. Sc. with Physics Honours from Bethune College, University of Calcutta in 2001 with 72.0% marks and university rank 15th.
- Completed Higher Secondary with Science group from Bethune College, W. B. Council of Higher Secondary Education in 1998 with 82.7% marks.
- Completed Madhyamik from R. K. S. M. Sister Nivedita Girls' School, in 1996 with 85.5 % marks.

Scholarship/Awards:

- GATE Scholarship in 2004 with percentile 90.14.
- National Scholarship in 2001 for the results in Physics Honours.
- Best Paper Award in Internation Conference on Information Technology (ICIT), 2007

Teaching Experience:

1. Working as a co-teacher in M.Tech Computer Science course in Indian Statistical Institute from July, 2006-till date.

2. Worked as Full-time Lecturer in Department of Computer Science and Engineering in Techno India College (Salt Lake) under WBUT from Aug, 2005 – June, 2006.

3. Worked as Part-time Lecturer in Department of Computer Science in Bethune College under University of Calcutta from Aug, 2005 – July, 2006.

Affiliations and Professional Activities

- Student Member, IEEE

- Member, International Association of Engineers (IAENG)

- Member, The Association of Computer Electronics and Electrical Engineers (ACEEE)

- Served as a Reviewer for IEEE Transactions on VLSI Systems, the journal IET Computers & Digital Techniques, and for several IEEE conferences VLSID'09, VDAT'09, VDAT'07, ICCTA'07, ICIT'07 etc.

- Member and serving as Joint Secretary, Women In Engineering (WIE), IEEE Calcutta Section.

Research Experience:

- Research Fellow (Institute Scholar) in Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata from July, 2006 – till date

  - Senior Research Fellow – Research post submission of Ph.D. Thesis
    -- July, 2011 – till date
  - Senior Research Fellow – Research towards Ph.D. Thesis
    -- July, 2008 – July, 2011
  - Junior Research Fellow -- Research towards Ph.D. Thesis
    -- July, 2006 – July, 2008.

  My research interest includes VLSI design optimization, meta-heuristic techniques and security issues.

- Technical Experiences during research:

  - List of Softwares used for research in VLSI:

    (i) Xilinx, VPR for FPGA
    (ii) DAIC, IC station and Calibre (from Mentor Graphics) for ASIC
    (iii) FastCap (for parasitic extraction)
    (iv) Atalanta (for test generation), fsim (for simulation).

  - Training attended:

    (i) CUDA Training & GPU Processing by the engineers of NVDIA
    (ii) DAIC, ICStation & Calibre from Mentor Graphics by the engineers of Coreel Technologies, Bangalore.

List of Publications:

Journal Publications:

1. Debasri Saha, Susmita Sur-Kolay, Secure Public Verification of IP Marks in FPGA Design through a Zero-Knowledge Protocol, *IEEE Transactions on VLSI (TVLSI) Systems* (In press), 2011.

2. Debasri Saha, Susmita Sur-Kolay, Robust Intellectual Property Protection of VLSI Physical Design, *Journal of IET Computers and Digital techniques, Vol 4, No. 5*, pp. 388-399, 2010 (available in IEEE Xplore).

3. Debasri Saha, Susmita Sur-Kolay, SoC: A Real Platform for IP Reuse, IP Infringement and IP Protection, *Journal of VLSI Design*, special issue '*CAD for Gigascale SoC Design and Verification Solutions'*, Hindawi Publishing Corporation, *USA*, vol 2011, article id 73195, 2011, (available in ACM portal).

4. Pritha Banerjee, Debasri Saha, Susmita Sur-Kolay, Cone based Placement for FPGAs, *Journal of IET Computers and Digital techniques*, vol 5, no. 1, pp. 49-62, 2011 (available in IEEE Xplore).

5. Debasri Saha, Susmita Sur-Kolay, Robust Verification of Public Marks in FPGA Design through a Zero-Knowledge Protocol, *Intl. Journal of Recent Trends in Engineering, Academy Publishers, Finland,* vol 1, no.1, pp. 168-172, 2009.

6. Debasri Saha, Parthasarathi Dasgupta, Susmita Sur-Kolay, Samar Sen Sarma, A novel scheme for IP Security in VLSI Physical Design, *Intl. Journal on Computer Science and Information Technology (IJCSIT),* vol 1, pp 58-67, 2007.

7. Rajat K. Pal, Debasri Saha, Samar Sen Sarma, A memetic Algorithm for Computing a Nontrivial Lower Bound on Number of Tracks in Two-Layer Channel Routing, *Journal of Physical Sciences* (ISSN: 0972-8791)*,* vol. 11, pp. 199-210, 2007.

Conference Publications:

1. D. Saha, Susmita Sur-Kolay, Pre and Post Fabrication Protection for DFM Enhanced Layout, In *Proc. IEEE Latin American Symposium on Circuits and Systems* (LASCAS), 2011.

2. D. Saha, Susmita Sur-Kolay, A Unified Approach for IP Protection across Design Phases in a Packaged Chip, In *Proc. IEEE International. Conference. on VLSI Design*, 2010 (VLSID), pp. 105-110.

3. D. Saha, Susmita Sur-Kolay, Secure Leakage-Proof Public Verification of IP Marks in VLSI Physical Design, In *Proc. IEEE Computer Society Annual Symposium on VLSI* (ISVLSI), Tampa, Florida, 2009, pp 169-174.

4. D. Saha, Susmita Sur-Kolay, Encoding of Floorplans through Deterministic Perturbation, In *Proc. IEEE International Conference on VLSI Design* (VLSID), 2009, pp 315-320.

5. D. Saha, Susmita Sur-Kolay, An Analytical Approach to Direct IP Protection of VLSI Floorplans, In *Proc. IEEE Intl. Conference on Industrial and Information System* (ICIIS), 2008.

6. D. Saha, Susmita Sur-Kolay, Fast Robust Intellectual Property Protection for VLSI Physical Design, In *Proc IEEE International Conference on Information Technology* (ICIT), 2007, pp 1-6. (Best paper award).

7. D. Saha, Pritha Banerjee, Susmita Sur-Kolay, Fast I/O Pad Placement in FPGAs, *Proc. of IEEE VLSI Design and Test Symphosium* (VDAT), 2007, pp. 152-161.

8. D. Saha, Parthasarathi Dasgupta, Susmita Sur-Kolay, Samar Sen Sarma, A novel scheme for encoding and watermark embedding in VLSI Physical Design for Intellectual Property Protection, In *Proc. International Conference on Computing: Theory and Application* (ICCTA'07), 2007, pp 111-116.

9. D. Saha, Watermarking Graph Coloring Problem, In Proc. *IEEE WIE National Symposium on Emerging Technologies* (WieNSET), 2007.

10. D. Saha, Rajat K. Pal, Samar Sen Sarma, A Memetic Algorithm for Refinement of Lower Bound of Number of Tracks in Channel Routing Problem, *IFIP International Federation for Information Processing, Vol. 228, Intelligent Information Processing III*, 2006, pp. 307-316.