VLSI 2005: Program Matrix for Technical Sessions and Industry Forum

	CRYSTAL Combined	**Crystal East**	**Hall Color Codes**	**Mandarin**	**Banquet Lawns**
	Crystal Central	**Crystal West**		**Incognito**	**Break**
	January 3, 2005				
9:00	Inauguration of Conference			Free	Free
9:30	Inaugural Keynote Address			Free	Free
10:30	Inauguration of Technical Exhibition			Free	Free
10:45	Morning Tea				
11:15	1A: Test I	1B: Physical Design	1C: Embedded Systems	1D: Low Power	1E: Industry Forum
13:15	Lunch				
14:30	2A: Formal Verification	2B: Nanotechnology and Biochips	2C: Synthesis I	2D: RF and Mixed Signal	2E: Industry Forum
16:30	Afternoon Tea				
17:00	Monday Afternoon Plenary Session			Free	Free
18:30	Break				
19:00	Monday Banquet Speech			Free	Free
20:00	Dinner				
	January 4, 2005				
8:30	Tuesday Morning Keynote Session			Free	Free
10:30	Morning Tea				
11:00	3A:Signal Integrity and Crosstalk	3B: Process Variation	3C: Design Methodology	3D: Placement and Routing	3E: Industry Forum
13:00	Lunch				
14:15	4A: Test II	4B: Analog	4C: Architecture	4D: Power Estimation and Low Power Design	4E: Industry Forum
16:15	Afternoon Tea				
16:45	Panel Discussion			Free	Free
18:15	Break				
18:45	Conference Speeches & Awards			Free	Free
19:30	Tuesday Banquet Speech			Free	Free
20:30	Dinner				
	January 5, 2005				
7:30	Breakfast			Free	Free
8:30	India Semiconductor Association Event				
9:30	Wednesday Morning Keynote Session			Free	Free
10:30	Morning Tea				
11:00	5A: Interconnect	5B: Synthesis II	5C: Power-aware design and Thermal Issues	5D: Technology	5E: Industry Forum
13:00	Lunch				
14:15	Wednesday Afternoon Plenary Session			Free	Free
15:45	Afternoon Tea				
16:15	6A: Test III	6B: Algorithms and Applications	6C: Posters	6D: Posters and RSF	6E: Industry Forum

VLSI 2005: Program Matrix for Industry Forum

	CRYSTAL Combined		**Hall Color Codes**		**Crystal Central**
	Mandarin		**Banquet Lawns**		**Crystal East**
	Incognito		**Break**		**Crystal West**
Session	**January 3, 2005**	**Session**	**January 4, 2005**	**Session**	**January 5, 2005**
1E		**3E**		**5E**	
11:15	Introduction to Industry Forum	**11:00**	Centilium	**11:00**	Magma-DA
11:25	Cadence	**11:20**	CoWare	**11:20**	Virage Logic
11:45	Intel	**11:40**	Interra Systems	**11:40**	eInfochips
12:05	Mentor Graphics	**12:00**	Tensilica	**12:00**	Xilinx-CMC
12:25	Texas Instruments	**12:20**	TranSwitch	**12:30**	National Instruments
12:45	Agere Systems	**12:40**	Softjin	**12:40**	Govt. of India
13:15	Lunch	**12:50**	Alumnus Software	**13:00**	Lunch
		13:00	Lunch		
2E		**4E**		**6E**	
14:30	nSys	**14:15**	Alliance Semiconductors	**16:15**	Adv. VLSI Design Lab - IIT, KGP
14:50	Synopsys	**14:35**	Trident Techlabs	**16:35**	Atrenta
15:10	LogicVision	**14:55**	Mechatronics	**16:55**	Zenasis
15:30	Natsem	**15:15**	Open-Silicon	**17:15**	Panel: Industry/Academia
15:50	Sequence Design	**15:35**	Infineon		
16:00	CG-CoreEl	**16:15**	Afternoon Tea		
16:30	Afternoon Tea				

VLSI 2005: Program Matrix for Tutorials

	January 6, 2005			
9:00	T1: Power-Aware reliable microprocessor design	T2: High-Speed Interconnect Technology: On-Chip and Off-Chip	T3: Testing Nanometer Integrated Circuits: Myths, Reality and the Road Ahead	T4: SoC Design Methodology: A Practical Approach
10:30	Morning Tea			
11:00	T1	T2	T3	T4
12:30	Lunch			
13:30	T1	T2	T3	T4
15:00	Afternoon Tea			
15:30	T1	T2	T3	T4
	January 7, 2005			
9:00	T5: Test Methodologies in the Deep Submicron Era - Analog, Mixed-Signal and RF	T6: Recent Advances in Verification, Equivalence Checking & SAT-Solvers	T7A: Compact MOSFET Models for Low Power Analog CMOS Design.	T8: Architectural, System Level and Protocol Level Techniques for Power Optimization for Networked Embedded Systems
10:30	Morning Tea			
11:00	T5	T6	T7A	T8
12:30	Lunch			
13:30	T5	T6	T7B: Physics and Technology: Towards Low-Power DSM Design	T8
15:00	Afternoon Tea			
15:30	T5	T6	T7B	T8