Optimizing SoC Manufacturability

Yervant Zorian
Virage Logic Corp
Outline

- Nanometer trends
- IP manufacturability challenges
- Optimization loops
- Examples in embedding manufacturability in IP cores
- Conclusions
Introduction

- **Cost**
  - reduce semiconductor development/fabrication expense and improve manufacturing yield

- **Time-to-Volume**
  - short time to market and short product lifecycle
  - faster yield optimization impacts market entry time and bottom line

- **Quality**
  - production of high quality manufactured silicon
Nanometer Trends

- Number of transistors
- Mixed technologies
- Shrinking geometries
- Process layers
- New process material
- High performance
Nanometer Impact

- Miniaturization and High Performance result in
  - Finer and denser semiconductor fabrication
  - Increased susceptibility
  - Increased defectivity
  - Lower manufacturing yield and reliability

- Observed as
  - Defect density
  - Realistic Faults
  - Timing problems
  - Transient or Soft Errors
IC Realization Flow
IC Realization Flow

IP Design \rightarrow \text{Characterization}
IC Realization Flow

- IP Design
- SoC Design
- Characterization

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IC Realization Flow

IP Design → SoC Design → Production Ramp Up → Characterization
IC Realization Flow

1. IP Design
2. SoC Design
3. Production Ramp Up
4. Volume Fabrication
5. Characterization
IC Realization Flow

- IP Design
- SoC Design
- Production Ramp Up
- Volume Fabrication
- Test Assembly Packaging
- Characterization

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IC Realization Flow

- IP Design
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- In-Field
- Characterization
- Failure Analysis

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Yield vs TTV Curve

Yield Assessment (%)

Design  Production Ramp Up  Volume

Fab Yield Optimization

Yield Learning Curve
Yield vs TTV Curve

Design Yield Optimization

New Yield Learning Curve

Fab Yield Optimization

Yield Learning Curve

Design
Production Ramp Up
Volume

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Yield vs TTV Curve

- Design Yield Optimization
- Yield Learning Curve
- New Yield Learning Curve
- Fab Yield Optimization

Yield Assessment (%) vs Time (TTV)

Design  Production Ramp Up  Volume

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Yield vs TTV Curve

Yield Assessment (%)

Design Yield Optimization
New Yield Learning Curve
Yield Learning Curve
Fab Yield Optimization

Design Production Ramp Up Volume

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Yield vs TTV Curve
1. Yield Learning Challenge

- Semiconductor process evolving and introducing new material and techniques
  - result in new generation of yield limiting factors
- Small geometries
  - result in devices more susceptible to systematic and random defects and higher defect densities per layer
- Increased time-to-market pressure
  - result in chip volume production at lower yield level
- Disaggregated semiconductor industry
  - result in F-IP providers assuming yield optimization responsibility
- Need IP validation and yield prediction and optimization for each new design (IP and SoC)
2. Embedded Memory Challenge

![Bar chart showing area share of memory and logic from 1999 to 2014. The chart indicates the percentage of area used for memory, reused logic, and new logic over different years. The chart includes a forecast for 2014.]

Source: SIA, ITRS 2000

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2. Embedded Memory Challenge

![Graph showing memory yield as a function of memory size.](image)

- **Memory Yield (without redundancy)**
- **Memory Yield with redundancy**

### Key Metrics:
- **Width of die in mm:** 12.00
- **Height of die in mm:** 12.00
- **Defect density for logic in # per sq. in.:** 0.4
- **Defect density for memory in # per sq. in.:** 0.8
- **Process technology:** 0.13 μm

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3. Mask Cost Challenge

- Mask cost is doubling with every new process node
  - increase Structured ASIC and FPGA competitiveness
  - cause fewer ASIC design starts

Source: Dataquest, Virage Logic estimates
4. Failure Analysis Challenge

- Traditional physical failure analysis steps -
  - Fault localization
  - Silicon de-processing
  - Physical characterization and inspection
- Small geometries result in –
  - Finding smaller more subtle defects
  - Tighter pitches require greater spatial resolution
  - Backside analysis due to metal layers & flip-chip
- Need to gather failure data using diagnosis IP and analyze obtained data by off-chip fault localization methodologies and tools
5. High Performance Challenge

- Increased performance require increased accuracy for proper resolution of timing signals
- Semiconductor on-chip speed improved 30% per year, test accuracy improved 12% per year
  - Tester timing errors approaching cycle time of faster device
  - Yield loss due to tester inaccuracy (extra guard-bending performed at test stage)
- Need for measuring and analyzing time specifications using embedded timing probes with high accuracy
6. Transient Error Challenge

- Smaller geometries and reduced power supplies result in reduced noise margins
- Soft errors, timing faults, crosstalk are major signal integrity problems
- SoC needs self correcting, i.e. embedded robustness, engine in order to resist to this challenge
Optimization Loops

- Need for advanced optimization solutions
- Introduced at different stages of chip realization flow
- Optimization loops – comprised of three steps
  - Detection, Analysis, Correction
- Three step loops either reside completely off-chip, partially on-chip/off-chip or embedded on-chip
- Examples of yield optimization feedback loops
Yield Optimization Loops

- IP Design
- SoC Design
- Production Ramp Up
- Volume Fabrication
- Test Assembly Packaging
- In-Field
- Characterization
- Failure Analysis

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Yield Optimization Loops

1. IP Design
2. SoC Design
3. Production Ramp Up
4. Volume Fabrication
5. Test Assembly Packaging
6. Failure Analysis

- Detection
- Analysis
- Correction
Yield Optimization Loops

- Detection
- Analysis
- Correction
Yield Optimization Loops

- Detection
- Analysis
- Correction
Yield Optimization Loops

1. Detection (D)
2. Analysis (A)
3. Correction (C)

Steps:
1. IP Design → Characterization
2. SoC Design → Characterization
3. Production Ramp Up → Characterization
4. Volume Fabrication → Failure Analysis
5. Test Assembly Packaging → Failure Analysis
6. In-Field → Failure Analysis

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Yield Optimization Loops

1. IP Design -> Characterization
2. SoC Design -> Production Ramp Up
3. Production Ramp Up -> Volume Fabrication
4. Volume Fabrication -> Test Assembly Packaging
5. Test Assembly Packaging -> Failure Analysis
6. Failure Analysis -> In-Field
7. In-Field -> Characterization

- Detection
- Analysis
- Correction
Multiple Functional IP (F-IP) types have been absorbed into single SoC design
Infrastructure IP in SoC

- Transparent to normal functionality of SoC (not functional IP)
- Ensures manufacturability and lifetime reliability of SoC
- Basic types of Infrastructure IP include:
  - IP for process monitoring
  - IP for testing
  - IP for diagnosis and debug
  - IP for repair
  - IP for characterization & measurement
  - IP for robustness and fault tolerance
Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
- External equipments and sensors
Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
  - External equipments and sensors
  - Embedded I-IP on Wafer
Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
  - External equipments and sensors
  - Embedded I-IP on Wafer
  - Embedded I-IP at SoC level
Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
  - External equipments and sensors
  - Embedded I-IP on Wafer
  - Embedded I-IP at SoC level
  - Embedded I-IP distributed over F-IP
Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
  - External equipments and sensors
  - Embedded I-IP on Wafer
  - Embedded I-IP at SoC level
  - Embedded I-IP distributed over F-IP
  - Embedded I-IP integrated into F-IP

- Resource partitioning and I-IP at multiple levels
- Examples of Embedding I-IP to create optimization loops
1. Embedded Process Monitor IP

1. IP Design
2. SoC Design
3. Production Ramp Up
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5. Test Assembly Packaging
6. In-Field

- Detection
- Analysis
- Correction

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1. Embedded Process Monitor IP

- Passing DRC does not guarantee high yield
- D-component of feedback loop is I-IP
  - Monitor process characteristics
  - Collect device attributes
- Known as: test vehicle or test die
- Process Monitor IP used during process development and/or later during production
- Process Monitor IP may be test die (full chip), scribe or embedded IP in SoC
1. Embedding Process Monitor IP

- Test die
- Product Die
- Process development
  I-IP
- Drop-in test die with scribe
- Scribe only
- Product die with embedded IP
1. Embedded Process Monitoring IP

- Use information and knowledge about process to predict yield of a given design (IP or SoC) before it is committed to silicon (A-component)
- Identify weekest links in design
  - Block, IP, layer, design structures
- Yield Optimization: improve design (IP or SoC) by modifying week links at GDS level (C-component)
1. Predicting IP Yield
1. IP Validation

- Standard test flow - memory
  - Parametrics
  - Functionality (March Pattern) across Vdd and Temp
  - Read Margin Characterization across Vdd and Temp
  - Stress Tests
  - Clock to Qout (Access Time) across Vdd and Temp
  - Power Measurement (Read/Write) across Vdd and Temp
  - Standby Current Characterization (Iddq) across Vdd and Temp
1. IP Validation

- Advanced Test Flow - memory
  - Active and Standby power trend
- OPC Simulation
  - Optical Proximity Correction and Contour
- DFM Examples
  - Design For Manufacturing
- DFR Example
  - Design For Reliability
  - NBTI (Negative Bias Temperature Instability) in PMOS
2. Embedded Test & Repair IP

- Detection
- Analysis
- Correction
2. Manufacturing Cost

- **Barriers**
  - **Cost**
    - $3-7 Million equipment cost
    - 40% of manufacturing cost
  - **Access**
    - Providing test access increases die size

[Image of a flowchart showing the stages of production, including memory tester, laser repair, logic tester, and packaging.]
2. I-IP for One Time Repair

- External Memory tester need eliminated
- External bit map storage eliminated
- External redundancy analysis software eliminated
- High yield achieved because of integrated solution
2. I-IP for Multi-Time Repair

- External repair equipment eliminated
- Overall manufacturing cost reduced
- Efficiency of repair increased (FVT corner conditions repaired)

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2. Example SoC
2. I-IP Effect on Yield & Reliability

- Type and amount of redundancy
- Fault detection & location algorithm
- Redundancy allocation algorithm
- Repair Methodology
- Reconfiguration mechanism
2. Time-to-Market: Development

- Pre-Integrated F-IP and I-IP into a single IP autonomous entity
- Interoperability
- Use of standard interface to I-IP, such as P1500
3. Functional Re-programmability

- Frequent functionality changes
  - New algorithms implementation
  - Functional revisions
- Design Fabric for Structured ASICs
- FPGA conversion for high volume designs
3. Metal Programmable Logic

- Reduce cost of design re-spin by 30-70%
- Decrease manufacturing turn-around-time
- No change in design flow or design tools
  - Conventional EDA tools
3. Metal Programmable Logic

- Initial Placement and Routing
- Remove metal layers and contacts
- Atomic Base Cells remain
- Re-synthesize and place new cells
- New functionality in same area
3. Embedded Diagnosis IP

IP Design → Characterization

SoC Design → Production Ramp Up

Production Ramp Up → Volume Fabrication

Volume Fabrication → Test Assembly Packaging

Test Assembly Packaging → Failure Analysis

Failure Analysis → In-Field

- Detection
- Analysis
- Correction
4. Embedded Diagnosis IP

- Need to gather failure data using diagnosis IP and analyze obtained data by off-chip fault localization methodologies, tools and equipment
- Leverage same infrastructure IP for test, silicon debug and diagnosis
- Integrated Silicon Debug Solution comprised of -
  - Generate embedded test & diagnosis IP
  - Integration embedded test & diagnosis IP
  - Failure data from diagnosis IP analyzed off-chip for fault localization
4. Conventional Diagnostics

- Traditional physical failure analysis steps
  - Test until fault detected
  - Fault localization
  - Silicon de-processing
  - Physical characterization and inspection
- 130-nm and 90-nm geometries
  - Finding smaller more subtle defects
  - Tighter pitches require greater spatial resolution
  - Backside analysis due to metal layers & flip-chip
4. Embedded Diagnosis IP

- IP includes diagnostic and failure analysis capabilities
- Dedicated diagnostic capabilities
  - Error monitoring
  - Stop-on-fail
  - Serial access
  - Fault Insertion
- Test modes for margining, speed binning
5. Embedded Timing IP

IP Design → Characterization

SoC Design

Production Ramp Up

Volume Fabrication

Test Assembly Packaging → Failure Analysis

In-Field

- Detection
- Analysis
- Correction
5. Embedded Timing IP

- Very stringent timing specification
- Difficulty in obtaining accurate measurements using external instrumentation
- Embedded timing IP [Tabatabaei 02] comprised of
  - Multiple high speed probes
  - Embedded control core directs probes and transfers information to timing processor for analysis
- Yield gain obtained due to accurate measurement
5. Yield Gain due to Timing IP

- **BAD CHIP**: Not accepted
- **GOOD CHIP**: Accepted per DAC

- **Increased Tolerance**

- **Yield Improvement**

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6. Embedded Robustness IP

- Detection
- Analysis
- Correction
The error bars account for the range of supply voltage. The SER increases exponentially at 2.1-2.2 decades/volt, e.g., 200X in 2005.
6. Soft Error Risk

A 0.13µm design offers **40X** more performance than 0.25µm...

... but is **40X** more prone to Soft Errors
6. Robustness IP for Memories

- Standard ECC architecture provides single bit repair and adds extra delay to each read and write operation.
6. Robustness IP for Logic

Source: iRoC
Conclusions

- Leverage IP design and manufacturing for higher yield and reliability to create silicon aware IP
- Leverage IP design for cost reduction and Time-to-Volume Acceleration
- Infrastructure IP may require external support, automated tools and equipment
- Optimization loops leveraged at different product realization steps during design, fabrication, test and in-field
- Collaborative environment is necessary to achieve Yield, Quality and TTV goals
THANK YOU FOR YOUR ATTENTION